【DESCRIPTION】

【TITLE】

TIME-INTERLEAVED BAND-PASS DELTA-SIGMA MODULATOR

【TECHNICAL FIELD】

The present invention relates to a time-interleaved bandpass Δ-Σ modulator (hereinafter, referred to as "a delta-sigma modulator"). More particularly, this invention relates to a delta-sigma modulator includes a plurality of channel blocks, of which the phase of the lock frequencies are different to each other, so as to reduce a clock frequency.

【BACKGROUND ART】

A delta-sigma modulator generally includes a lowpass modulator and a bandpass modulator. The lowpass modulator is used for audio devices, while the bandpass modulator is used for radio communication. The delta-sigma modulator may be composed of a continuous-time circuit or a discrete-time circuit, with reference to Fig. 1a and Fig. 1b. A bandpass delta-sigma modulator in Fig. 1b samples the intermediate-frequency (IF) as much as four times, and removes quantization noise (this is referred to as shaping). In the modulator, because the noise is shaped at the input signal within the desired band, high signal-to-noise ration (SNR) can be achieved at the input signal on the desired band.

A bandpass delta-sigma modulator, which is implemented by a

continuous-time circuit (see Fig. 1a), has an advantage that it can operate in high frequency band. However, it also has a disadvantage that a user must tune a center frequency. In the case of a bandpass delta-sigma modulator in Fig. 1b, which is embodied by discrete-time circuit, such as a switched capacitor circuit, however accurate and reliable it may be, it cannot be operated on the commonly used high frequency IF band, because it must use a clock frequency four times higher than the input signal.

【DISCLOSURE OF INVENTION】

This invention has been developed to avoid the drawbacks of the conventional delta-sigma modulator. Therefore, it is an object of the present invention to provide a time-interleaved bandpass delta-sigma modulator which is capable of directly performing analog-to-digital conversion even on high frequency IF band of radio communication systems, by innovatively lightening requirements of a clock frequency and settling time.

As such, a main concept of this invention is that it performs the same function as the conventional discrete signal bandpass delta-sigma modulator shown in Fig. 1b. However, it can be constituted by only adders and comparators which include a plurality of channel blocks without delay means' (z^{-2} or 2-delay), thereby reducing the requirements of a clock frequency and a settling time, depending on the number of channel blocks.

Fig. 2a and Fig. 2b show an example of the conventional delta-sigma modulator, modified from one in Fig. 1b. It is noted that a device in Fig. 2a

performs the same function as a device in Fig. 1b, and Fig. 2b is a functional equivalent view against Fig. 2a.

In Figs. 2a and 2b, input signal x enters a first adder 11. Output u of he first adder 11 is fed-back to the first adder 11 through a 2-delay, and enters a second adder 13 through a 2-delay 12. Output v of the second adder 13 is fed-back to the second adder 13 through a 2-delay 14, and simultaneously enters a comparator 15. Output y of the comparator 15 is again fed-back to the first adder 11 and the second adder 13 through the 2-delays, so that the analog input signal x can be converted to the digital output signal y. However, the conventional delta-sigma modulator must sample the input signal by using a clock frequency four times higher than the input signal, and therefore, it cannot be operated in the commonly used high frequency IF band, which has been discussed above.

To overcome this problem, the present invention delta-sigma modulator uses a plurality of channel blocks without the delay means'. The channel blocks are included in a dashed box 20 of Fig. 2b without delay means'. Clock frequency of the respective channel blocks is reduced in inverse proportion to the number of channel blocks, and phase difference of the clock frequency becomes 1/5 on every channel blocks. For example, if the number of channel blocks is 5, the clock frequency decreases to 1/5.

Therefore, according to the present invention, an input signal is inputted to the first adder according to an each channel block's clock frequency, and an n'th channel block's output u_n of the first adder is inputted to the first adder and the second adder of an (n+2)'th channel block, and an n'th block's output v_n of

the second adder is inputted to the second adder of an (n+2)'th block, and an output y_n that passes an n'th block's comparator is inputted to the first adder and the second adder of an (n+2)'th block. Therefore, a modulator of the present invention receives output of the each block's comparator sequentially and makes the final output y, which is analog-to-digital converted output signal. Therefore, when supposing the number of channel blocks is N, wherein a phase difference between n'th channel block and (n+1)'th channel block is sampled to 1/N of the clock frequency.

【BRIEF DESCRIPTION OF DRAWINGS】

The above and other objects, features and advantages of the present invention will become more apparent from the following description when taken in conjunction with the accompanying drawings, in which:

Figs. 1a and 1b are schematic diagrams of a conventional delta-sigma modulator,

Figs. 2a and 2b are schematic diagrams modified from Fig. 1b,

Fig. 3 is a schematic diagram of one embodiment of the present invention,

Fig. 4 is a timing diagram of the present invention,

Fig. 5 is a detailed view of a channel A in Fig. 3, and

Figs. 6a-6c shows another embodiment of the present invention.

【Preferred Embodiments for Carrying out the Invention】

Preferred embodiments of a time-interleaved delta-sigma modulator

according to the present invention will be described below with reference to the accompanying drawings.

Fig. 3 shows a delta-sigma modulator of the present invention, which is constituted by five channel blocks. Fig. 4(a) is a timing diagram of the conventional delta-sigma modulator shown in Fig. 1b, and Fig. 4(b) is a timing diagram of the delta-sigma modulator of the present invention, shown in Fig. 3. Fig. 5 shows a detailed circuitry of channel A shown in Fig. 3, which is constituted by switched capacitors.

In Fig. 3, each the channel block is implemented by a dashed box in Fig. 2b. Also, all of the channel blocks have the same constitution, except the phase of the clock frequency. The phase differences of the clock frequency of each the channel block are depicted in Fig. 4(b). The phase difference of the clock frequency of the neighbouring channel block is 1/5 of a period. Because of the phase differences, input signals sequentially enter the channel block, respectively, and the adder output of the n'th channel block is changed at $\Phi_{n,2}$. At this time, since the adder output of the n'th channel block should reach the steady state condition before the start of $\Phi_{n+2,2}$ clock of the (n+2)'th channel block, the required settling time can be reduced to 1/4 and the required clock frequency can be reduced to 1/5, compared to a single channel block.

Fig. 5 is a specific circuit diagram of channel block A of the 5-channel block delta-sigma modulator implemented by switched capacitors, which is comprised of a first adder 11', a second adder 13', and a comparator 15'. Fig. 5 shows one example of the present invention, and therefore, the scope of the inventive concept of this invention should not be limited to the diagram shown in

Fig. 5.

With reference to Figs. 3 and 5, the input signal x is sequentially inputted to the first adder of each channel block, in accordance with the phase of each the clock frequencies. Then, the output u_A of the first adder 11', the output v_A of the second adder 13', and the output y_A of the comparator 15' are transferred to channel C. That is, the output u_A of the first adder 11' of channel A is inputted to both a first and a second adders of channel C, the output v_A of the second adder of channel A is inputted to the second adder of channel C, and the output y_A of the comparator 15' of channel A is inputted to both the first and the second adders of channel C.

In such a manner, in the case of Fig. 3, the outputs u_A, v_A, y_A of channel A are inputted to channel C and the outputs u_B, v_B, y_B of channel B are inputted to channel D, channel C to channel E, channel D to channel A, channel E to channel B, etc.

Resultantly, the output y of the 5-channel-block delta-sigma modulator shown in Fig. 3 is the same as the output of the conventional bandpass delta-sigma modulator shown in Fig. 1b. However, as shown in Fig. 4(a) and (b), the clock frequency of the 5-channel-block delta-sigma modulator is reduced to 1/5 compared to the conventional single channel block delta-sigma modulator, and the settling time of the 5-channel-block delta-sigma modulator is reduced to 1/4 compared to the conventional single channel block delta-sigma modulator. Therefore, the present invention can be implemented on a practical IF band by using switched capacitor circuits.

Although the number of channel blocks has been five(5) so far, it does

not need to be limited to this, of course. 7-channel-block, 9-channel-block, etc. are possible - odd numbers greater than or equal to five(5). It is noted that a circuit designer should trade off between in that, as the number of channel blocks increases, the clock frequency and settling time become decreased and the circuit becomes more complicated.

Figs. 6a and 6b shows another embodiment of the present invention, a time-interleaved delta-sigma modulator. In construction, the outputs u_n, v_n, y_n of an n'th channel block are inputted to a (n+3)'th channel block, in order to implement 4-dealy (z^{-4}) instead of 2-delay in Fig. 2a. In this case, the basic number of channel block is nine(9), and this 9-channel-block delta-sigma modulator has the clock frequency 1/9 of that of the conventional single channel block delta-sigma modulator, and it has the settling time 1/8 of that of the conventional single channel block delta-sigma modulator. For this embodiment, the number of channel blocks may be selected out of 5, 9, 11, 13, etc.

In Fig. 6c, (a) is a timing diagram of a single block delta-sigma modulator, and (b) is a timing diagram of a 4-delay 9-channel-block bandpass delta-sigma modulator. It can be noticed that the clock frequency is reduced to 1/9 and the settling time is reduced to 1/8 compared to the conventional single channel block delta-sigma modulator.

From the foregoing, although a conventional bandpass delta-sigma modulator implemented by switched capacitors cannot be operated on a high frequency IF band, since the clock frequency of the present invention can be significantly reduced, the present invention can be effectively performs analog-to-digital conversion even on high frequency IF band. Therefore, it increases

flexibility in a wireless communication system, and reduces the costs.

While the invention has been shown and described with reference to a certain embodiment to carry out this invention, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.